

Notice of References Cited	Application/Control No. 10/654,983	Applicant(s)/Patent Under Reexamination YASUDA ET AL.	
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U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-6,738,870 B2	05-2004	Van Huben et al.	711/150
	B	US-6,636,926 B2	10-2003	Yasuda et al.	710/305
	C	US-6,088,768 A	07-2000	Baldus et al.	711/141
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	K	US-			
	L	US-			
	M	US-			

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NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	"Performance evaluation of cache depot on CC-NUMA multiprocessors" by Hung-Chang Hsiao; Chung-Ta King (abstract only) Publication Date: 14-16 Dec. 1998
	V	"Computation/communication balance-point modeling in multiprocessors" by Hamacher, V.C. (abstract only) Publication Date: 22-24 Aug. 1999
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*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
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	U	"A novel approach to reduce L2 miss latency in shared memory multiprocessors" by Acacio, M.E.; Gonzalez, J.; Garcia, J.M.; Duato, J. (abstract only) Publication Date: 15-9 April 2002
	V	"Architectural support for uniprocessor and multiprocessor active memory systems" by Kim, D.; Chaudhuri, M.; Heinrich, M.; Speight, E." (abstract only) Publication date: March 2004
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